CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1-4. (canceled)

5. (original) A field programmable gate array (FPGA) comprising:

input and output data communication connections;

a serializer/deserializer circuit coupled to the input and output data communication connections; and

a logic array programmed to generate a test data pattern coupled to the output data communication connection, the logic array is further programmed to check a data pattern received on the input data communication connection while performing a built in self test operation.

6. (previously presented) The FPGA of claim 5 further comprises a digital clock manager circuit to generate a clock signal couplable to the logic array, wherein the digital clock manager circuit adds noise and jitter in a controlled manner in both programmable jitter amplitude and programmable jitter frequency to the clock signal during the built in self test operation.

7. (previously presented) The FPGA of claim 5 further comprises a digital clock manager circuit to generate clock signals couplable to the logic array, wherein the digital clock manager circuit creates frequency offsets and phase shift phases between the clock signals during test operations.

8. (original) The FPGA of claim 5 wherein the logic array is further programmed to insert cyclical redundancy check characters in the test data pattern.

9. (original) The FPGA of claim 5 further comprising a memory to store data indicating test operation results.

10. (original) A method of testing a high speed interconnect circuit of a field programmable gate array (FPGA) comprising:

generating a test pattern using programmed logic circuitry of the FPGA;

outputting the test pattern on an output connection;

coupling the test pattern to an input connection of the high speed interconnect circuit;

evaluating data received on the input connection using the programmed logic circuitry; and

storing data indicating a result of the evaluation.

11. (original) The method of claim 10 wherein the logic array is programmed to operate as a linear feedback shift register to provide a pseudo random bit stream as the test pattern.

12. (original) The method of claim 10 further comprises adding an error checking character to the test pattern prior to outputting the test pattern on the output connection.

13. (original) The method of claim 12 wherein evaluating the data received included evaluating the error checking character.

14. (original) A test system comprising:

a test circuit; and

a field programmable gate array (FPGA) coupled to the test circuit, wherein the FPGA comprises,

input and output data communication connections coupled together through the test circuit,

a serializer/deserializer (SERDES) circuit coupled to the input and output

data communication connections, and

a logic array programmed to generate a test data pattern coupled to the output data communication connection, the logic array is further programmed to check a data pattern received on the input connection while performing a built in self test operation.

15. (original) The test system of claim 14 wherein the FPGA comprises a memory to store data indicative of a result of the check of the received data pattern.

16. (original) The test system of claim 15 wherein the test circuit accesses the FPGA memory to determine an error status of the FPGA.

17. (previously presented) A method of testing a serializer/deserializer (SERDES) circuit of a field programmable gate array (FPGA) comprising:

programming a logic array of the FPGA;

generating a test pattern using the programmed logic array of the FPGA;

outputting the test pattern on an output connection of the SERDES circuit;

externally coupling the test pattern to an input connection of the SERDES circuit;

using the programmed logic array, evaluating data received on the input connection;

storing data indicating a result of the evaluation in a memory circuit of the FPGA; and

re-programming the logic array to perform an end user application.

18. (original) The method of claim 17 wherein the logic array is programmed to comprise a pseudo random bit generator function, or other stress or test pattern.

19. (previously presented) The method of claim 17 further comprises:
generating a clock signal using a digital clock manager (DCM) circuit; and
coupling the clock signal to the SERDES circuit.

20. (previously presented) The method of claim 17 further comprises:
generating transmit and receive clock signals using a digital clock manager (DCM) circuit, wherein the digital clock manager circuit creates frequency offsets, jitter magnitude and jitter frequency and phase shift phases between the transmit and receive clock signals; and
coupling the clock signal to the SERDES circuit.